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09/478,812
**BOX AF**

AF/2815

OIPE JC95 JAN 22 2002 PATENT & TRADEMARK OFFICE

RECEIVED JAN 25 2002 TC 2800 MAIL ROOM

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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|---|---|
| In the Patent Application of | Group Art Unit: 2815 |
| Yukiyasu SUGANO et al. | |
| Serial No. 09/478,812 | Examiner: E. Lee |
| Filed: January 7, 2000 | |
| For: PROCESS FOR PRODUCING THIN FILM SEMICONDUCTOR DEVICE AND LASER IRRADIATION APPARATUS | |

## TRANSMITTAL OF APPEAL BRIEF

**BOX AF**
Commissioner for Patents
Washington, D.C. 20231

Sir:

Three copies of an Appellant's Brief on Appeal for the above-referenced application are being filed herewith. The Commissioner is hereby authorized to charge $320.00 to Deposit Account 18-0013 to cover the requisite fee under 37 C.F.R. 1.16 or 1.17 which may be required, or to credit any overpayment.

The Notice of Appeal for this application was filed on November 21,2001.

Respectfully submitted,

Ronald P. Kananen
Registration No. 24,104

DATE: January 22, 2002

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15/ appeal Brief J. Steptoe 2/2/02

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In the Patent Application of

Yukiyasu SUGANO et al.

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For: PROCESS FOR PRODUCING THIN FILM SEMICONDUCTOR DEVICE AND LASER IRRADIATION APPARATUS

Group Art Unit: 2815

Examiner: E. Lee



**APPEAL BRIEF**

Commissioner of Patents
**BOX AF**
Washington, DC 20231

Sir:

This is an Appeal Brief under Rule 192 appealing the final decision of the Primary Examiner dated June 21, 2001 ("Paper No. 10"). Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

## I. Real Party in Interest

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventors and recorded by the U.S. Patent and Trademark Office at reel 010792, frame 0182.

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## II. Related Appeals and Interferences

There are no appeals or interferences related to the present application of which the Appellants are aware.

## III. Status of Claims

The Application as filed contained claims 1 to 74. After canceling claims in view of a restriction requirement and other amendments, only claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 are pending on appeal. No amendments have been made to the claims since the mailing of Paper No. 10.

## IV. Status of Amendments

Claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63 to 65, and 73 to 74 were initially examined. Claim 64 has been canceled, and the claims have been amended since initial examination. Following the issuance of Paper No. 10, Appellants filed a Response to Final Office Action on September 19, 2001, and the Notice of Appeal was thereafter filed. Thus, the claims as presented in the Appendix represent all amendments that were made up until issuance of Paper No. 10.

## Summary of the Invention

A first aspect of the present invention includes a thin film semiconductor device. The device includes a semiconductor thin film (e.g. layer 5, Fig. 7D), with a gate insulating film (combined film layers 2 and 3) accumulated on one surface thereof (lower surface of layer 5). A gate electrode (1) is accumulated on the semiconductor thin film (5) via the gate insulating thin film (2 and 3). The semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon (layer 4 in Fig. 7B, page 39, lines 13 to 15). An energy beam is applied to a prescribed region, and a cross sectional shape of the energy beam is adjusted with respect to the prescribed region to irradiate the prescribed region in a single shot (page 10, lines 14 to 19; page 39, line 23 to page 40, line 6).

As shown in Fig. 11, plural units may be formed on the substrate (0). In this case, the irradiation step is conducted so that the substrate (0) is irradiated intermittently in order to convert the amorphous or polycrystalline material (4) to a polycrystalline material (page 45, lines 6 to 19). Further, a cross sectional shape of the energy beam is adjusted with respect to each unit to irradiate one or two or more units at a time by a single shot

irradiation (page 45, last line to page 46, line 3).

At the time of formation, the amorphous silicon or polycrystalline silicon (4) has a first particle diameter; and after being irradiated with the energy beam, the semiconductor thin film (4) is converted to polycrystalline silicon (5) having a larger particle diameter than the first particle diameter (page 48, lines 10 to 16).

Regarding the laser irradiation step, such step may be performed by irradiating the prescribed region of the substrate one or more times with a pulse of laser light having a constant cross sectional area and an emission time width from upstand to downfall of 50 ns or more (Fig. 23A, page 69 lines 6 to 11). Further, a desired change to the energy intensity of the laser light from upstand to downfall of the pulse is applied to said polycrystalline silicon (page 67, line 16 to page 68, last line).

According to the first embodiment of the invention, a thin film transistor (112, Fig. 8) is integrated and formed in a prescribed region by using the semiconductor thin film (5) thus converted to polycrystalline silicon as an active layer (page 43, lines 13 to 17). Due to the energy beam irradiation, characteristics of the thin film transistor are made uniform.

A second aspect of the invention involves a display device

(Fig. 8, page 42, lines 12 to 15). The device includes a pair of substrates (101, 102) adhered to each other with a prescribed gap, and an electrooptical substance (103) maintained in the gap (page 42, lines 15 to 18). One of the substrates (102) includes a counter electrode, the other substrate (101) includes a pixel electrode (111) and a thin film transistor (112) driving the pixel electrode (111). The thin film transistor (112) includes a semiconductor thin film and a gate electrode accumulated on one surface of the semiconductor thin film through a gate insulating film as described above regarding the first aspect of the invention. The formation steps regarding the semiconductor thin film and the active region are also the same as described above.

A third aspect of the invention involves a thin film transistor having a laminated structure (Fig. 7, page 38, lines 17 to 19). The transistor includes a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating thin film, according to the same construction as defined above regarding the first aspect of the invention. Further, the formation steps described above are the same, although in this embodiment, the semiconductor thin film is accumulated by alternately repeating the film forming step and the

irradiation step, without exposing the substrate to the air (Fig. 14, page 52, lines 9 to 12).

A fourth aspect of the invention involves a display device as described above regarding the second aspect of the invention, using the method described above regarding the third aspect of the invention. According to the principle of accumulation of the semiconductor thin film, a semiconductor thin film (2A in Fig. 19A to F) is formed by forming a layer of about 20 nm amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate (page 59, lines 5 to 8). The film (2A) is irradiating according to a prescribed region of the substrate (1A) with laser light having a prescribed cross sectional shape to convert to polycrystalline silicon having a larger particle diameter than the first diameter as described above. Then, additional semiconductor thin films are accumulated by alternately repeating the film forming step, where each additional formed film is about 1 nm (page 60, lines 19 to page 61, line 4).

As stated above, with regard to any of the aspects of the invention, it is preferred that during the irradiation steps, the substrate is maintained in a non-oxidative atmosphere (page 27, lines 12 to 13). Further, in one embodiment it is preferred that the irradiation step is performed under conditions where the substrate is uniformly heated (page 26,

lines 16 to 20). In another embodiment, the substrate is cooled to a temperature lower than room temperature during the irradiation step (page 26, line 24 to page 27, line 4).

## VI. References of Record

In the final rejection of Paper No. 10, the Examiner relied upon the following prior art against claims 1 to 7, 9 to 22, and 24 to 26:

(1) U.S. Patent No. 5,352,291 ("Zhang");

(2) U.S. Patent No. 5,798,744 ("Tanaka").

## VII. Issues

In light of the final rejection in Paper No. 10, the issues presented on this appeal are:

(1) whether claims 11, 17, 27, 39, 53, 63, 73 recite obvious subject matter, as these claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhang;

(2) whether claims 12, 18, 28, 40, 54, 65, and 74 recite obvious subject matter, as these claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhang in view of Tanaka.

## VIII. Grouping of Claims

All of the claims stand or fall together. The reasoning for the grouping of the claims is evident in light of the following arguments.

## IX. Arguments

As conceded by the Examiner, the limitation in each of the claims regarding the height of the layers of amorphous polysilicon film is not taught or suggested by either the Tanaka or the Zhang patent. The Zhang process is usable for making polycrystalline silicon film from an amorphous semiconductor film which is not disclosed throughout the Zhang specification to be any smaller than 100 nm. The Examiner asserts that it would have been an obvious matter of design choice to have a significantly smaller amorphous silicon layer, as such a change merely constitutes a change in size. To this point, Applicant disagrees with the Examiner.

The reason that a significantly thinner amorphous semiconductor layer than that which is disclosed by Zhang is more than a mere change in size lies in the manner by which the claims establish that the semiconductor device is produced. It is understood that the process limitations in the claims are not given patentable weight to the claims unless the process limitations somehow ascribe structure to

the product made by the process. However, it is also important to note that the process steps explain the significance of other product limitations. In the present case, the smaller thickness of the amorphous semiconductor layer is more significant than a mere change in size because, as the claims recite, the irradiation that the layer is subjected to is a bulk irradiation that is conducted in such a manner that a cross sectional shape of an energy beam is adjusted with respect to the region by a single shot irradiation.

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Because the cross sectional shape of the energy beam is pertinent to the thickness of the semiconductor layer, the process within the product claim, while not yielding additional patentable weight to the claims, does exhibit a rationale that supports the argument that a person of ordinary skill in the art would not find motivation in the Zhang patent, or the Tanaka patent for that matter, for arriving at the claimed product. There is no teaching or suggestion in Zhang or the remaining cited prior art references that the Zhang process could be applied to a thinner amorphous film. In fact, the present specification clearly teaches that the problems associated with the Zhang process (merely eliminating hydrogen from amorphous semiconductor films using heat without laser processing) are overcome by the presently claimed

invention. Further, Zhang fails to teach or suggest that the cross sectional shape of an energy beam should be adjusted with respect to an irradiated region, e.g., a significantly thinner region than that disclosed by Zhang.

The examiner has the initial burden of demonstrating that all the claimed features of the invention are taught by the prior art. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Where the examiner relies on a single reference under § 103, as is the case with the limitation of the presently claimed 30 to 80 nm amorphous semiconductor layer, it is insufficient to merely state that it would be obvious, or a mere matter of design choice, to modify the disclosure of that reference to include the features of the claimed invention. In re Mills, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990). "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." M.P.E.P. § 2143.03. (emphasis added). Accord. M.P.E.P. § 706.02(j).

It is appealed that the Board not uphold this type of a rejection in which the examiner simply alleges that the relevant feature of a claimed invention is a mere "design choice." Such a statement "is a conclusion, rather than a reason." Ex parte Garrett, 1986 Pat. App. LEXIS 8, 4 (BPAI 1986). "To imbue one of ordinary skill in the art with

knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effects of a hindsight syndrome." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (quoting W.L. Gore & Assoc. v. Garlock, Inc., 220 USPQ 303, 312-13 (Fed. Cir. 1983)). Because the evidence set forth above weighs strongly against the limitation of a 30 to 80 nm amorphous semiconductor layer being a mere matter of design choice, the rejections of the pending claims should not be sustained.

It is briefly pointed out that the Tanaka patent fails to make up for the limitations discussed above, to which the teachings of the Zhang patent are deficient. The Tanaka patent is only relied upon for display device features, and makes no mention of a thickness of an amorphous semiconductor layer that is crystallized.

X. Conclusion

In view of the foregoing, it is submitted that the final rejection of claims 11 to 12, 17 to 18, 27 to 28, 39 to 40, 53 to 54, 63, 65, and 73 to 74 is improper and should not be sustained. Therefore, a reversal of the Final Rejection in Paper No. 10 is respectfully requested.

Respectfully submitted,

DATE: January 22, 2002

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**APPENDIX**

Claims on Appeal

11. A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film is formed by forming a 30to 80 nm layer 0f amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, and irradiating said substrate with an energy beam to convert said semiconductor thin film to polycrystalline silicon having a larger particle diameter than said first particle diameter,

a thin film transistor is integrated and formed in a prescribed region by using said semiconductor thin film thus converted to polycrystalline silicon as an active layer, and

a cross sectional shape of said energy beam is adjusted with respect to said region to irradiate said region at a time by a single shot irradiation, so that characteristics of said thin film transistor is made uniform.

12. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said

substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a first particle diameter on said other substrate, and irradiating said other substrate with an energy beam to convert said semiconductor thin film to polycrystalline silicon having a particle diameter that is larger than said first particle diameter,

a thin film transistor is integrated and formed in a prescribed region by using said semiconductor thin film thus converted to polycrystalline silicon as an active layer, and

a cross sectional shape of said energy beam is adjusted with respect to said region to irradiate said region at a time by a single shot irradiation, so that characteristics of said thin film transistor is made uniform.

17. A thin film semiconductor device comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said

semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, on which plural units are formed, and intermittently irradiating said substrate, so as to convert to polycrystalline silicon having a particle diameter that is larger than said first diameter,

a cross sectional shape of said energy beam is adjusted with respect to said unit to irradiate one or two or more units at a time by a single shot irradiation, and

a thin film transistor is integrated and formed in said units thus subjected to irradiation at a time.

18. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, on which plural units are formed, and intermittently irradiating said substrate, so as to convert said semiconductor thin film to polycrystalline silicon having a larger particle diameter than said first diameter,

a cross sectional shape of said energy beam is adjusted with respect to said unit to irradiate one or two or more units at a time by a single shot irradiation, and

a thin film transistor is integrated and formed in said units thus subjected to irradiation at a time.

27. A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating thin film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, and irradiating a prescribed region of said substrate with laser light having a prescribed cross sectional shape to convert said semiconductor thin film to polycrystalline silicon having

a larger particle diameter than said first diameter, and

said semiconductor thin film is accumulated by alternately repeating said film forming step and said irradiation step without exposing said substrate to the air.

28. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a layer of about 20 nm amorphous silicon or polycrystalline silicon having a first particle diameter on a substrate, and irradiating a prescribed region of said substrate with laser light having a prescribed cross sectional shape to convert to polycrystalline silicon having a larger particle diameter than said first diameter, and

said semiconductor thin film is accumulated by alternately repeating said film forming step, where each additional formed film is about 1 nm, and said irradiation

step without exposing said substrate to the air.

39. A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on a substrate, and irradiating a prescribed region of said substrate one or more with a pulse of laser light having a constant cross sectional area and an emission time width from upstand to downfall of 50 ns or more, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time, and

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon.

40. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate

comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on said other substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width from upstand to down fall of 50 ns or more, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time, and

a desired change to said energy intensity of said laser light from upstand to downfall of said pulse is applied to said polycrystalline silicon.

53. A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film is formed by forming

a 30 to 80 nm layer of non-single crystal silicon on a substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more with maintaining said substrate in a non-oxidative atmosphere, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.

54. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on said other substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more with maintaining convert said non-single crystal

silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.

63. A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on a substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more under conditions in that said substrate is uniformly heated, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to polycrystalline silicon at a time.

65. A display device comprising a pair of substrate adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrate comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor comprises a semiconductor thin film and a gate electrode

accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on said other substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more under conditions in that said other substrate is uniformly heated, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.

73. A thin film transistor having a laminated structure comprising a semiconductor thin film, a gate insulating film accumulated on one surface thereof, and a gate electrode accumulated on said semiconductor thin film through said gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on a substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more under conditions in that said substrate is cooled to a temperature lower than room temperature, so as to convert

said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.

74. A display device comprising a pair of substrates adhered to each other with a prescribed gap, and an electrooptical substance maintained in said gap, one of said substrates comprises a counter electrode, the other substrate comprises a pixel electrode and a thin film transistor driving said pixel electrode, and said thin film transistor comprises a semiconductor thin film and a gate electrode accumulated on one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on said other substrate, and irradiating a prescribed region of said substrate once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more under conditions in that said other substrate is cooled to a temperature lower than room temperature, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.